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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,771	01/10/2002	Peter I. Majewicz	D/A1294;690_010500_US(PAR	8318

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Geza C. Ziegler, Jr.
Perman & Green, LLP
425 Post Road
Bridgeport, CT 06430

EXAMINER	
COLILLA, DANIEL JAMES	
ART UNIT	PAPER NUMBER
2854	

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,771	MAJEWICZ ET AL.	
	Examiner	Art Unit	
	Dan Colilla	2854	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-6* is/are allowed.

6)☒ Claim(s) *7-12 and 14-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 17 is rejected under 35 U.S.C. 102(b) as being anticipated by Matsushita.

Matsushita discloses an LED array including two chips 1 placed adjacent to each other with each chip 1 including a plurality of LED's 2. Each end LED 2a and 2b has an electrode 3a and 3b, respectively, that is inward biased toward the center of the chip 1 from the center of the LED 2 thus forming a light center or centroid closer to the edge of the chip (see paragraph [0014], lines 10-12 of the machine translation and Figure 2b of Matsushita). Viewing Figures 1 and 2b of Matsushita and noting the centroid position of Figure 2b it can be seen that the pitch of the pixels is constant.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita in view of Kahen et al.

With respect to claim 7, Matsushita discloses the claimed structure except for the wire bond pads and the specific pitch of approximately 21.2 μm. Matsushita discloses a plurality of LED chips 1 butted together with a gap between adjacent LED's 2 to form and array as shown in Figure 1 of Matsushita. Also disclosed are center electrodes 3 extending from each LED 2. Matsushita is silent on how the electrodes are connected to the chip 1. However, wire bond pads are a well-known structure used for creating circuitry and the use of such structure would have been obvious to one of ordinary skill in the art for the advantage minimizing the circuitry and allowing easy attachment of electrical components to the circuitry. The LED's are adapted for emitting light and as a result will have a centroid over the LED. Further disclosed by Matsushita is an LED 2a and 2b at each respective end of the chips 1 which have an electrode 3a and 3b, respectively, that is biased inward toward the center of the chip. Thus resulting in a centroid emitted light from each end LED 2a and 2b that is positioned closer to an outer edge of the chip 1 (Matsushita, lines 9-11 of the English translated constitution). While Matsushita does not disclose the pitch of approximately 21.2 μm the ideal pitch would have been obvious to one of ordinary skill in the art through routine experimentation or calculation.

Similarly, with respect to claim 10 the optimal dimensions between the chip edges and LED edges and between adjacent chips could have readily been determined by one or ordinary skill in the art through routine experimentation.

With respect to claim 11, Matsushita discloses that the arrow head shown in Figure 2b of Matsushita indicates the light center (centroid) of the LED 2a. This position is to the right of the center of the LED 2a.

5. Claims 8, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita in view of Kahen et al. as applied to claims 7,, 9-10 above, and further in view of applicant's admittance of prior art.

With respect to claims 8 and 10, Matsushita in view of Kahen et al. discloses the claimed structure except for the gap between chips being 5 μm. However, applicant's discloses on page 7, line 6-7, that the prior art shown in Figure 2 is known to have a gap of 5 μm between chips 22a and 22b. Furthermore, it would have been obvious to one of ordinary skill in the art to determine the optimal spacing of the chips and LED's through ordinary routine experimentation.

With respect to claim 9, applicant also discloses that the chips shown in Figure 2 of applicant's disclosure have 1200 SPI (page 7, lines 3-4 of applicant's disclosure).

6. Claims 12, 14, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita et al.

With respect to claim 12, Matsushita discloses the claimed high resolution LED array except for the specific pitch of approximately 21.2 μm. Matsushita discloses a plurality of LED chips 1 placed end to end with a gap between as shown in Figure 1 of Matsushita. Also disclosed are center electrodes 3 extending from each LED 2. The LED's are adapted for emitting light and as a result will have a centroid. Figure 1 of Matsushita shows that each chip 1 has a pair of LED's on respective ends of each chip 1 that has an electrode 3a and 3b respectively that is inward biased. While Matsushita does not disclose a pitch of 21.2 μm, it would have been obvious to one of ordinary skill in the art would to determine the ideal pitch through routine experimentation or calculation.

With respect to claims 14, the specific dimensions this claim would have been obvious to one of ordinary skill in the art through routine experimentation or calculation.

Similarly, the dimension recited in claims 18 and 20 would have been obvious to one of ordinary skill in the art through routine experimentation or calculation.

7. Claims 15-16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita, as applied to claims 12 and 14 above, and further in view of applicant's admittance of prior art.

With respect to claim 15, Matsushita in view of Kahen et al. discloses the claimed structure except for the gap between chips being 5 μm. However, applicant's discloses on page 7, line 6-7, that the prior art shown in Figure 2 is known to have a gap of 5 μm between chips 22a and 22b. Furthermore, it would have been obvious to one of ordinary skill in the art to determine the optimal dimensions of the chips and LED's through ordinary routine experimentation.

With respect to claims 16 and 19, applicant also discloses that the chips shown in Figure 2 of applicant's disclosure have 1200 SPI (page 7, lines 3-4 of applicant's disclosure).

Allowable Subject Matter

8. Claims 1-6 are allowed.

Response to Arguments

9. Applicant's arguments filed 2/5/04 have been fully considered but they are not persuasive of any error in the above rejection.

With respect to claim 17, applicant's amendment to the claim is functional language which, is not necessarily improper, it is not given any weight when determining patentability of the claim. The language of the amendment is an intended method of making the LED array and does not further limit the structure as required in an apparatus claim.

Similarly, the amendment to claims 7 and 12 also do not add any further structure to the claims.

With respect to applicant's arguments regarding Figure 2 as admitted prior art, the spacing of 5 μm is known and desirable and in view of the patent to Matsushita, one of ordinary skill in the art would recognize the ability to create such a spacing of LED's for a fine resolution.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

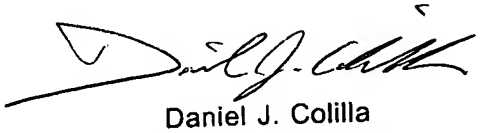
however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Colilla whose telephone number is (571)272-2157. The examiner can normally be reached Tues.-Fri. between 7:30 am and 6:00 pm. Faxes regarding this application can be sent to (703)872 - 9306.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Hirshfeld can be reached at (571)272-2168. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 4, 2004



Daniel J. Colilla
Primary Examiner
Art Unit 2854